Special Meeting 2

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Quantum Computing

Applications

- Factorization
  - Shor [25] $\mathcal{O}(\log N^3)$ vs. GNFS [20] $\mathcal{O}(\exp\sqrt{\frac{64}{9}}\log N^{\frac{1}{3}}\log\log N^{\frac{2}{3}})$
- Unstructured search
  - Grover [9] $\mathcal{O}(\sqrt{N})$ vs. linear search [14] $\mathcal{O}(N)$
- Simulation of quantum systems
  - Molecular interaction [1]
- Quantum artificial intelligence
  - Perovskite structure prediction [19]
  - Climate modelling [29]

$\Rightarrow$ **Near exponential speedup for certain applications**

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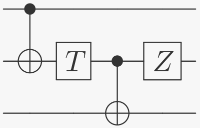
Quantum Circuits [21]

- Analagous to classical logic gates
- But **reversible**
- Input is reconstructable from output
- Gates are unitary operators
- Not all gates have classical counter part (eg. Hadamard)



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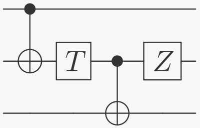

What is the catch?

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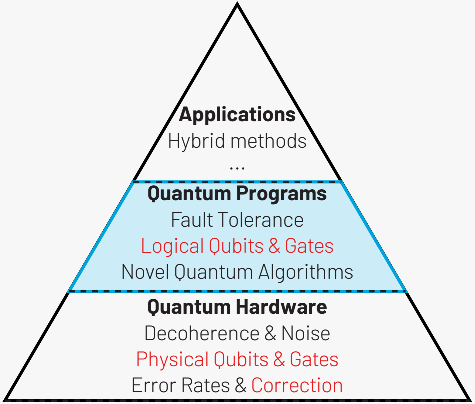
Quantum Computing

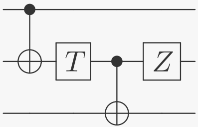
- **Ressource restrictions**:
  - 127 logical qubits [6]
  - up to ≈ 5000 logical gates
  - short coherence time ($80[\mu s]$ to $1[ms]$) [26]
- **Error correction**:
  - noise drives gate error rate [28]
  - limits the number of usable gates
  - overhead varies by an order of magnitude for different gates [24]
- **Quantum computing limited to artificial problems**



$\Rightarrow$ **Architecture-independent QC optimization**

QC Optimization

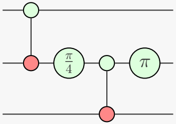
- Infinite universal gate sets
- Infinite gate commutation rules
- Equivalence verification computational expensive



$\Rightarrow$

ZX Calculus [2, 3]

- 8 generators
- 9 well defined rewriting rules
- Rewriting rules preserve semantics

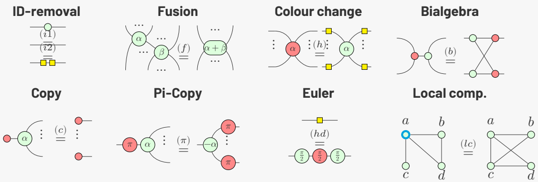


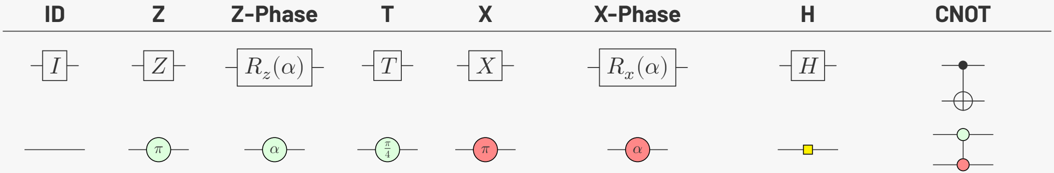
$\Rightarrow$ **State-space for combinatorial optimization is (infinitely) large**

ZX calculus

Diagrammatic Reasoning Framework

- Every QC can be expressed as a ZX diagram [30]
- **Semantic preserving rewriting rules**
- Circuit extraction is # P-hard [4]
- Applied for QC optimization and verification





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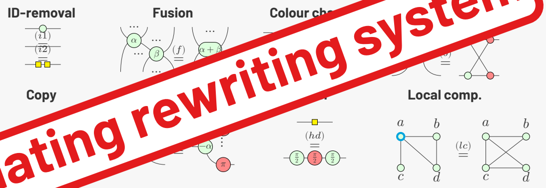
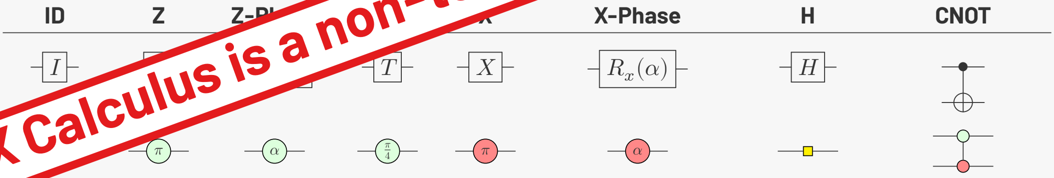
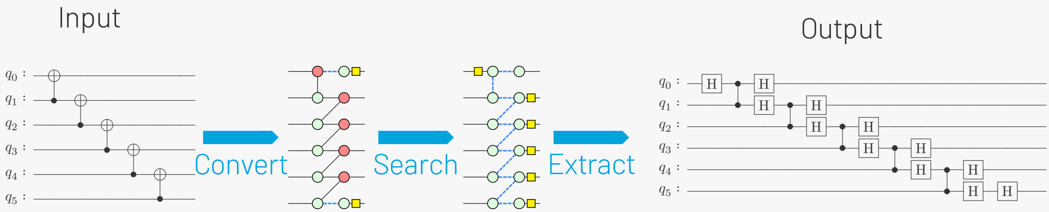


ZX Calculus is a non-terminating rewriting system



Optimization Pipeline



Experimental Setup

Challenges

- Non-termination $\rightarrow$ select efficient pruning conditions
- Failed circuit extraction $\rightarrow$ compute metrics on ZX diagram; ensure graph-likeness
- High-memory requirement $\rightarrow$ open question

Benchmark

- 100 standard quantum circuits
- 1.5 hour global timeout
- Pruning conditions:
  - No colour cycle
  - No spider unfusion
  - Rule bundling
- DFS & IDDFS
- Connectivity change takes precedent over spider count

Results

T-gate reduction

DFS

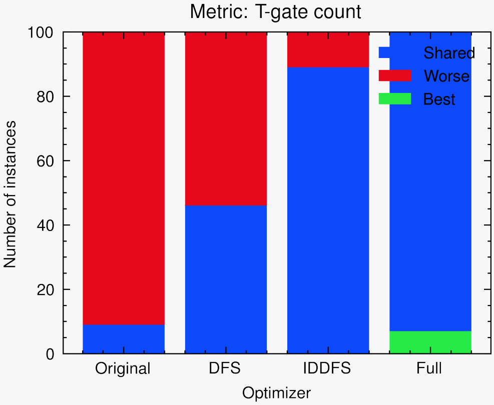
- reduces T-gate count by $\approx 10\%$
- equates Full reduce on 46% of the instances

IDDFS

- reduces T-gate count by $\approx 26\%$
- equates Full reduce on 89% of the instances

Full reduce [13]

- reduces T-gate count by $\approx 27\%$
- always leads to the best result



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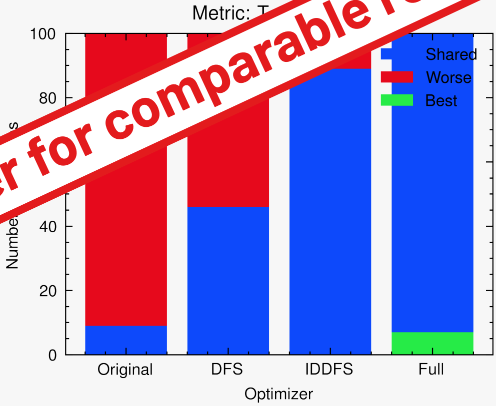


Orders of magnitudes slower for comparable results

DFS

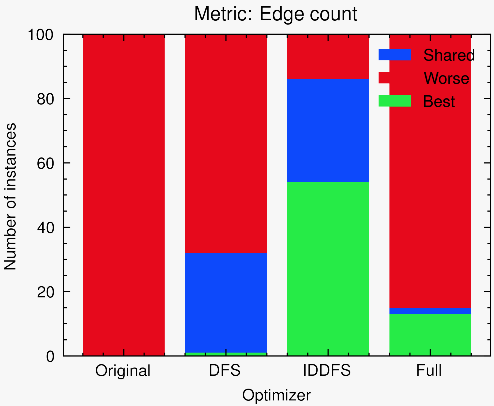
- reduces Edge count by $\approx 11\%$
- best solution on 32% of the instances

IDDFS

- reduces Edge count by $\approx 22\%$
- best solution on 86% of the instances
- comparable to SOTA algorithms that target Edge count (29% reduction) [27]

Full reduce

- not designed for edge count reduction
- reduces Edge count by $\approx 2\%$
- best solution on 15% of the instances



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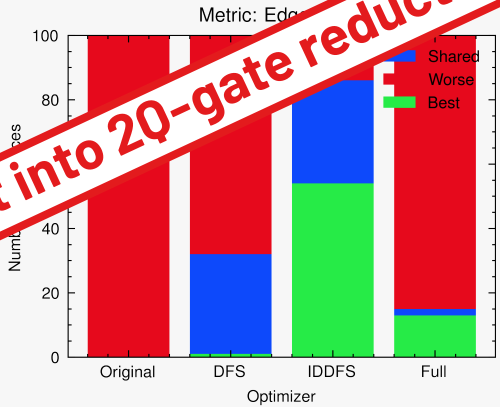

How to translate Edge count into 20-gate reduction?

Challenges

- Non-termination → select efficient pruning conditions
- Failed circuit extraction → compute gflow or cflow
- High-memory requirement → open question
- Slow → Improve heuristic
- Improved results → consider all rules; allow temporary worse metrics
- Balanced circuits → Multiobjective optimization

Improved Heuristic

- No rule has a vanishing probability $\rightarrow$ Limited-Discrepancy Search inefficient
- Restrict worsening of metrics by $x\%$ (new pruning condition) [27, 10]
- Compute flow properties instead of circuit extraction
- Allow rule reversal [27, 22, 17]
  1. verify cflow (computationally cheap)
  2. verify gflow only if cflow not present (computationally expensive)
- Order rules by:
  1. spider degree $\deg$
  2. edge count N_e
  3. spider count N_{spiders}

$$h : \{\textbf{ZX}, r \in \textbf{R}\} \Rightarrow \{(x_i, v \in \textbf{ZX}), (x_{i+1}, w \in \textbf{ZX})...\| x, i \in \mathbb{N}\}$$

$$x_i = \deg \cdot (\Delta N_e + \Delta N_{\text{spiders}})$$

Composite Score

$$S = \sum_i w_i \cdot \frac{m_i^{\text{current}}}{m_i^{\text{input}}}$$

- w_i: weight for metric i and $\sum_i w_i = 1$
- m_i: value of metric i

$$S = S_{\text{indep}}^{\text{ZX}} + S_{\text{arch}}^{\text{ZX}} + S_{\text{indep}}^{\text{QC}} + S_{\text{arch}}^{\text{QC}}$$

$\Rightarrow$ **There is not one metric that defines a good ZX diagram or QC**

Composite Score

ZX	Architecture-independent
N_e	Number of diagram edges
N_{he}	Number of Hadamard edges
N_{spiders}	Spider count
N_{phases}	Number of non-zero phase spiders
N_T	Number of spiders with phase $\pi/4$
ZX	**Architecture-dependent**
$\deg_{\text{avg}}$	Average degree of spiders

QC	Architecture-independent
G_{2Q}	Number of two-qubit gates
G_{1Q}	Number of one-qubit gates
T	T-count
T_d	T-depth
D	Logical circuit depth
Q	Number of logical qubits
C	Clifford count
QC	**Architecture-dependent**
G_{CS}	Number of SWAP added
D_{phys}	Physical circuit depth
Q_{phys}	Physical qubits
E_{total}	Estimated total gate error
F_{expected}	Circuit fidelity

Multiobjective optimization

SOTA

- Lexiographic optimization of T-gates (full reduce) followed by two-qubit gates or two-qubit depth $\rightarrow$ same starting point
- Tree search allows temporary worsening of a metric for better results in the future [27, 10]
- Genetic algorithm that targets two-qubit gates and circuit depth, but only approximately [7]
- Combination of tree search with reenforcement learning is effective and scales well for larger circuits (future work?) [17]

Simulated Annealing

- adjust probability by rule order heuristic
- IDDFS for tree exploration
- keep metric score and rule order heuristic in memory
- prune solutions that worsen the composite metric by more than $x\%$

Proposed Roadmap

- implement improved rule selection heurisitc
- new pruning condition for worse circuits based on composite metric
- select suitable parameters for composite metric
- balance computational requirement of metric with quality of solution
- use multiobjective optimization techniques such as simulated annealing to improve speed

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